TE ECS Sem V 'C' scheme Winter 2025 13/11/25

(Time: 3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. Attempt any four questions
(a) Define Preemptive and Non-Preemptive Scheduling (5)
(b) Explain Superscalar Architecture. (5)
(c) Explain memory interleaving techniques (5)
(d) Define CPI, clock speed and MIPS. (5)
(e) Compare CPU and GPU

2. (a) What is deadlock condition in OS? (10)
(b) Explain Register Organization in CPU (10)

3. (a) Explain Microprogrammed Control Unit in detail. (10)
(b) What is the necessity of cache memory? Explain set associative cache mapping. (10)

4. (a) Explain various pipeline hazards. Explain the performance metrics for instruction pipelines (10)
(b) Explain priority scheduling algorithm. For the given Priority Scheduling find average waiting time. (10)

Process	Arrival Time	Execution Time	Priority	Service Time
P0	0	5	1	0
P1	1	3	2	11
P2	2	8	1	14
P3	3	6	3	5

5 (a) Explain FIFO page replacement algorithm. Find out Miss ratio, Hit ratio for the following string using FIFO method. (10)
(Consider page frame size = 3)
4 , 7, 6, 1, 7, 6, 1, 2, 7, 2
(b) Write short note on Virtual Memory Management. (10)

6. (a) What is BUS? Explain it's types in detail. Explain BUS arbitration mechnism. (10)
(b) Explain Flynn's classification of computers. State Amdahl's Law with formula. (10)

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